REMARKS/ARGUMENTS

The Examiner's Action of September 27, 2005, has been received and reviewed by counsel for Assignee. In that Action the Examiner requested a new title, and a new title is provided herewith.

The Examiner also rejected claim 1 under 35 U.S.C. § 102 as anticipated. All other claims were rejected under 35 U.S.C. § 103 as obvious as being unpatentable over *Muckenhirn* (U.S. 2003/0168594) in view of enumerated other references.

By this response counsel has canceled all pending claims and submits herewith new claims 16-26 which correspond generally to the former claims, but rewritten to include additional features of Applicants' invention to thereby patentably distinguish the cited references.

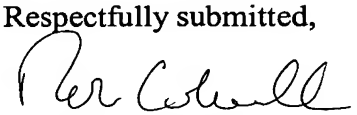
This invention relates to techniques for improving the manufacture of semiconductor devices or integrated circuits. In particular, test structures are formed on the same wafer as the actual circuits, and these test circuits are used to help assure that the layers formed on the semiconductor device are appropriately patterned. In the preferred embodiment a three-dimensional test structure is formed on the wafer and a relationship between that test structure and a process parameter used in forming the semiconductor device is determined. For example, the relationship of the test structure to a photolithographic patterning step is determined. See, e.g., the specification beginning on page 14 at line 20 and continuing through page 16 at line 22. A second corresponding relationship is determined between the varied process parameters and the measured features of the three-dimensional shape of a portion of the actual circuit pattern. Once the relationship of the circuit pattern to the process parameters and the relationship of the process parameters to the test structure is known, then the three-dimensional characteristics, typically measurements, performed on the test structure using the optical scatterometry apparatus as described, provides information about the actual circuit structure. In particular, the resulting information enables the manufacturing process to be monitored for operations which are not established with sufficient accuracy to the underlying structure, in which the photolithographic light source is improperly focused, etc. Even in circumstances where it is "too late" to fix the mistake, the cost of processing the wafer through the remaining manufacturing steps is avoided by virtue of the early detection of the mistake.

The *Muckenhirn* published application teaches tools for analyzing semiconductor structures, but it does not teach the particular technique of forming test structures as described and claimed in Applicants' claims. *Muckenhirn* appears to be primarily related to integrating two instruments within a single instrument so that an optical instrument such as a scatterometer and a feature-measuring instrument such as a scanning probe microscope are integrated into the same tool. There is no particular teaching noted by counsel as to the particular techniques described and claimed by Applicants. *Bendik et al.* in U.S. 6,673,638 teach the formation of a test pattern for monitoring changes in exposure conditions and thereby process management. The test structures appear to facilitate correct focusing on the wafer by virtue of employing wavefront features which determine whether the reticule is out of focus. *Singh* in U.S. 6,778,268 teaches an optical system for determining gate dimensions. By comparing signals associated with the gate to those previously stored from various measurements, the gate dimensions can be determined. *Yoshitake et al* in U.S. 2003/0121022 teaches management of an exposure process using optical scatterometry apparatus.

None of these references, taken singularly or in combination, however, teach calculating two relationships -- a first one between the test structure and a variation in process parameters, and a second one between the actual circuit structure and the test circuit structure and outside parameters.

Each of the independent claims now calls for this first and second relationship to be determined and used in controlling the semiconductor manufacturing process. Accordingly, counsel believes all of the claims are in appropriate form and patentably distinguish the cited art. If the Examiner believes a telephone conference would expedite prosecution of this application, he is invited to telephone the undersigned at 650-324-6303 (direct).

Respectfully submitted,



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